REMARKS

Applicants thank the Examiner for indicating that the references cited with the Information Disclosure Statement filed on July 11, 2003 have been considered.

However, with regard to the references cited with the Information Disclosure Statement filed on July 7, 2006, the Examiner has indicated that translations have not been submitted with the foreign references disclosed with the IDS, and has both initialed and struck through the entries for JP 1-133299, 1-223700 and JP 8-31196 on the form PTO/SB/08.

Applicants submit that the IDS is in compliance with the provisions of 37 CFR § 1.97. As the Examiner is aware, translations are not required for references not published in English; only a concise explanation of relevance, either in the specification or separately, is required. (37 CFR § 1.98(a)(3)(i)). As the Examiner is aware, where the information listed is not in the English language, but was cited in a search report or other action by a foreign patent office in a counterpart foreign application, the requirement for a concise explanation of relevance can be satisfied by submitting an English language version of the search report or action which indicates the degree of relevance found by the foreign office. MPEP § 609.04(a)III. Applicants submit that above references are concisely explained in the English translated portion of the Japanese Office Action submitted with the IDS.

Applicants have attached a new form PTO/SB/08 listing the above references and respectfully request that the Examiner initial the form indicating that the references have been considered.

Claim Rejections

Claims 1-7 and 9-15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,688,219 to Takemae ("Takemae") in view of U.S. Patent No. 5,307,356 to Fifield ("Fifield").

With regard to independent claim 1, the combination of Takemae and Fifield does not disclose or suggest at least wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data mask block and controlled by independent data mask signals as external signals, as recited in the claim.

Takemae is primarily directed to a memory device having redundant memory and parity checking capabilities, and merely discloses that the invention includes an error correcting circuit operatively connected to the memory cell array for receiving read data from a plurality of memory cells including a selected memory cell (column 2, lines 12-22). Fifield, simply discloses the use of a Hamming error correction code. Even if one of ordinary skill in the art at the time the invention was made had been motivated to combine the references, the combination would still not result in the claimed features. Therefore, claim 1 is patentable over the combination of Takemae and Fifield.

In the Response to Arguments, the Examiner alleges that features relied upon by Applicants as not disclosed in the references are not recited in the claim. Specifically, the Examiner alleges that the claim 1 does not recite " ... independent data masks controlled by independent data mask signals ... " **Applicants have amended claims 1 and 9.**

The last three lines of claim 1 recite "wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data mask block and controlled by independent data mask signals as external signals." Since the data mask signals independently control the 8-bit data, a plurality of error correcting code circuits, one for each 8 bits of data, is required. While Applicants' invention claims error correcting code circuits provided independently of each other for each data mask block controlled by a data mask signal, the combination of Takemae and Fifield fails to disclose or suggest independent data mask blocks controlled by independent data mask signals

Therefore, since the combination of Takemae and Fifield does not disclose or suggest at least wherein said error correcting code circuit comprises a plurality of divided error correcting code circuits provided independently of each other for each independent data mask block and controlled by independent data mask signals as external signals, claim 1 is patentable over the combined references.

Independent claim 9 contains features similar to the features contained in claim 1 and is therefore patentable for similar reasons. Claims 2-7 and 10-15, which depend from one of independent claim 1 and independent claim 9, are patentable at least by virtue of their dependencies.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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